Reliability of Ultra Fine-Pitch Flip Chip Assemblies Using Lead-free Alloys

Dr. Rainer Dohle – Micro Systems Engineering GmbH


This tutorial examines the reliability of ultra fine-pitch flip chip assemblies with lead-free solder bumps for which there are two major reliability aspects to consider: Thermo cycling performance and electromigration (EM). Isothermal aging and humidity should not cause significant problems, providing that suitable materials have been selected, see [1] and chapter "Results". First, dry heat storage, temperature humidity bias testing, and temperature cycling were conducted, showing excellent reliability of these ultra fine-pitch assemblies. Second, electromigration (EM) performance of the flip chip assemblies (with solder sphere sizes mentioned above) was investigated.

Experiment

The test coupons used in this study are specially designed flip chip packages. SAC305 Solder spheres with 40 µm, 50 µm, or 60 µm diameter were attached to silicon chips 10 x 10 x 0.8mm in size, using the wafer level solder sphere transfer process (often called "gang ball placement") and 30 µm SAC305 spheres using a laser based single-sphere process, respectively [2]. Even exotic solder compositions are readily accommodated using these methods.

Figure 1 shows the layout of the flip chip and the bumps on the chip. A circumferential daisy chain connection is integrated for each of the solder sphere sizes and each chip can be connected for online measurements during reliability or EM testing. The AlCu0.5 trace interconnection on the die is 1 µm thick, the Ni-P UBM 5 µm (with flash gold on top).

Fig 1: All-purpose test chips with 50 µm solder bumps (top) or 40 µm solder bumps (bottom). Solder spheres with 60 µm diameter would be placed at the outer row, solder spheres with 30 µm diameter at the 4th row.

Two different types of substrate were used for the experiments. On one hand, it was the aim of the substrate structuring that low-cost, standard processes of subtractive PCB technology be used. This meant that for passivation reasons, a solder mask had to be applied after etching the circuitry. As a final surface finish, ENIG was selected and the copper trace on the PCB is 9 µm thick, coated with 5 µm Ni
and flash gold. As shown in [3], the solder mask seems to have a negative effect on the long term reliability of the solder joints, when solder spheres with a diameter less than 50 µm are used. Because of this, a second test specimen based on thin film ceramic technology was employed, in order to overcome the limitations of the solder mask. The wettable areas (flash gold) of the thin film ceramic substrate are of high precision. The layout of the PCB and the layout of the thin film substrate are shown in figure 2.

![Fig 2: Layout of the test PCB with solder mask and the ceramic test coupon. During flip chip soldering, a circumferential daisy chain will be formed.](image)

The flip chips were placed onto the substrates using an automated assembly machine with 10 µm placement accuracy at 3 Sigma and reflowed after flux activation. The gap between chip and substrate was filled with high performance underfill material using a standard dispensing process and then thermally cured. Table 1 summarizes the employed tests.

**Table 1: Reliability tests conducted in this study.**

<table>
<thead>
<tr>
<th>Test</th>
<th>Method</th>
<th>Description</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EIA/JESD22-A101-C</td>
<td>Test with current through the daisy chain</td>
<td>85°C/85% relative humidity, 100 mA, 2000 hours</td>
</tr>
<tr>
<td>2</td>
<td>EIA/JESD22-A101-B</td>
<td>Voltage between two adjacent daisy chains</td>
<td>85°C/85% relative humidity, 3V, 2000 hours</td>
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<tr>
<td>3</td>
<td>DIN EN 60 068-2-14</td>
<td>Temperature cycling</td>
<td>-40°C/125°C 3057 cycles</td>
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<tr>
<td>4</td>
<td>MIL-STD 883H, method 1010.8 C.B.</td>
<td>Temperature cycling</td>
<td>-55°C/125°C 15000 cycles / 3000 cycles</td>
</tr>
<tr>
<td>5</td>
<td>MIL-STD 883H, method 1005.9</td>
<td>High temperature storage</td>
<td>125°C 1000/2000 hours dry heat</td>
</tr>
<tr>
<td>6</td>
<td>JEDEC JEP154</td>
<td>Electromigration</td>
<td>8kA/cm²/5kA/cm² T=125/100/28°C, 8000 hours</td>
</tr>
</tbody>
</table>

During EM testing, the daisy chains were connected to a constant current DC power supply. The failure criterion has been defined as an open in the daisy chain. After test 3 to 6, a few samples were ground and polished towards the center of the solder joints. These cross sections were then examined by SEM/EDX. The EM tests were done under the stress conditions shown in Tables 2 and 3.
Table 2: Test conditions for EM tests with PCBs.

<table>
<thead>
<tr>
<th>$\varnothing_{\text{sphere}}$ µm</th>
<th>$\varnothing_{\text{passivation}}$ µm</th>
<th>$T_{\text{oven}}$ °C</th>
<th>$T_{\text{chip}}$ °C</th>
<th>J kA/cm²</th>
<th>I mA</th>
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<tr>
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<td>60</td>
<td>125</td>
<td>187</td>
<td>8</td>
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<td>50</td>
<td>28</td>
<td>35</td>
<td>5</td>
<td>98</td>
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</table>

Table 3: Test conditions for EM tests with thin film ceramic.

<table>
<thead>
<tr>
<th>$\varnothing_{\text{sphere}}$ µm</th>
<th>$\varnothing_{\text{passivation}}$ µm</th>
<th>$T_{\text{oven}}$ °C</th>
<th>$T_{\text{chip}}$ °C</th>
<th>J kA/cm²</th>
<th>I mA</th>
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<td>125</td>
<td>128</td>
<td>8</td>
<td>57</td>
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The current density values are calculated by dividing the applied current by the area of the UBM metallization of the chip. The chip temperature $T_{\text{chip}}$ has been measured on the die surface above the current carrying daisy chain; the solder bump temperature ($T_{\text{bump}}$) was somewhat higher. The sample size was $n=12$ for each EM test.

Results

Figures 3 to 9 show the results for humidity temperature bias tests, high temperature storage, and temperature cycling.
Fig 3: Life test at 85 °C / 85 % relative humidity with a current flow of 100 mA through the daisy chain (PCB).

Fig 4: Test with a voltage of 3 V between two adjacent daisy chains at 85 °C and 85 % relative humidity (PCB).

Figure 5 shows the SEM image of a chip with 30 µm solder bump on thin film ceramic before and the element mapping for Ni, Sn, and Ag after 2000 hours isothermal high temperature storage at 125 °C. Energy-dispersive X-ray analysis (EDX) revealed that the IMCs gradually grew on both interfaces with similar thicknesses. Ni is effective as a diffusion barrier as can be concluded from the Ni and Sn distribution in the right picture. There is still ductile solder material in the center of the bump.
Fig 5: SEM image of a cross section of a flip chip with 30 µm solder spheres on thin film ceramic directly after reflow and underfill (left), Element mapping for Ni, Sn, and Ag for a flip chip with 30 µm solder spheres on thin film ceramic after 2000 hrs of thermal aging at 125 °C (right).

<table>
<thead>
<tr>
<th>Failure Rate in Dependance on the Number of Temperature Cycles (Chips with 60 µm solder spheres on PCB)</th>
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<tr>
<td>Number of temperature cycles -40 °C/+125 °C</td>
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<tr>
<td>Failure rate [%]</td>
</tr>
<tr>
<td>0 47 154 311 461 570 728 961 1041 1356 1623 1890 2140 2438 2737 3057</td>
</tr>
<tr>
<td>-40 °C/+125 °C</td>
</tr>
</tbody>
</table>

Fig 6: Failure rate for flip chips with 60 µm solder bumps on BT PCB during temperature cycling -40 °C/+125 °C.

Figure 7 shows a cross section of a flip chip with 50 µm solder bump on PCB after 2000 temperature cycles according to MIL-STD883H.

Fig 7: SEM picture from a cross section of a flip chip with 50 µm bump on BT PCB after 2000 temperature cycles -55 °C / +125 °C.
The single failure after 4268 temperature cycles can be considered as an early failure. Due to the only moderate CTE mismatch between chip and substrate and the excellent properties of the employed high performance underfill, the temperature cycling performance is very good. Flip chips with 30 µm on thin film ceramic showed no failures during 1000 temperature cycles between -55 °C/+125 °C (end of test). Figure 9 shows the element mapping for Ni, Sn, and Ag for a flip chip with 30 µm solder bump on thin film ceramic after 1000 temperature cycles according to MIL-STD883H (SE = secondary electrons). There is still ductile solder material in the middle of the bump.
As the bump size decreases, the ratio of solder volume to surface area decreases, thus the IMCs with similar thicknesses on both interfaces will constitute a larger portion of the bump. However, after high temperature storage or thermal cycling, we found still ductile solder in the center of all analyzed solder bumps, confirmed by EDX. Ductile material is especially advantageous if parts with a large mismatch of the coefficients of thermal expansion (CTE) are joined together.

After the EM experiments, the samples were ground and polished towards the center of the solder joint. Shown in figure 10 are typical cross-section images for flip chips with 60 µm solder bumps on thin film ceramic after EM testing. Interfacial intermetallic compounds in the solder bump joints were formed during reflow soldering already. The direction of electron flux is marked with small arrows in the images. The impact of the current crowding is apparent in the figures as indicated by the dissolution of IMC and UBM. Ni is seen within the bump, suggesting that Ni is driven into the solder bump by the electron flux. The migration direction of Ni is the same as the electron flow. No voids or cracks at the interface could be found, however. We contribute this to the lower chip temperature (about 154.4 °C) of the ceramic test coupons (due to better cooling) in comparison to the flip chips on PCB where the Joule heating generated by Al trace and bump structures elevated the test temperature much more. Therefore, with the same EM testing condition, the life time of the PCB test coupons must be shorter than the life time of the ceramic test coupons.

Backscatter Electron (BSE) image mode of scanning electron microscope (SEM) and optical micrographs (not shown here) indicate slight changes in the morphology only. EDX analysis revealed the movement of Nickel due to momentum transfer between conducting electrons and metal atoms [4]. The figures in the second row show a bump stressed with current in the opposite direction as in the top row.

The thinnest region of the UBM is located at the entrance of the current flow into the bump, where the current density has the highest value (current crowding). The extent of EM where the electron flow enters the UBM is therefore more severe than in other places in the metallization at the cathode side.

The 30 µm, 40 µm, and 50 µm solder bumps on thin film ceramic did not show strong EM effects because the bump temperature was lower than in the case of bumps with 60 µm diameter.
Figure 11 shows the void propagation at the cathode side, at which current crowding and Joule heating enhanced the EM phenomenon.

Shown in figure 12 are typical cross-sectional micrographs for flip chips with 60 µm solder bumps on PCB after EM testing. The direction of electron flux is marked with arrows in the images. As can be seen from these images, failures are caused by the growth of voids and cracks at either the UBM/solder interface at the chip side or the Ni/solder interface at the PCB side.

Fig 11: SEM image of a cross section of a flip chip with 60 µm solder spheres on PCB after EM test with 8kA/cm² at 125 °C oven temperature with end-to-end crack at the cathode side.

Fig 12: SE image (left) of a cross section of a flip chip with 60 µm solder spheres on PCB after 143 hours EM test with 8kA/cm² at 125 °C oven temperature (T_{chip} 187 °C). EDX mapping of this bump for Sn, Cu, and Ni (center) and for Ni (right picture). Photos in row 2 show the equivalent analysis for the opposite current direction.
The crack at the cathode side propagated completely through the solder joint (fig. 11+12), causing the connection to eventually fail. The UBM at the anode side is still faultless, as can be seen from the distribution of Ni and Sn in figure 12. The figures in the second row show a bump stressed with current in the opposite direction as in the figures in the top row.

The impact of the current crowding is obvious. Ni has been found within the solder bump (see figure 10 and 24), suggesting that Ni is driven into the solder bump by the electron flux. Electromigration caused atomic accumulation at the anode side, and vacancy condensation, UBM consumption, and void formation at the cathode side. It is noticeable that these voids were primarily generated in the current crowding region. It can be concluded that these voids did spread across the contact area over time and finally caused failure of the solder joint by crack propagation, compare figure 11.

Joule heating due to current flow develops a non-uniform temperature distribution in the solder bumps, which could induce thermomigration, driven by temperature gradients, if large enough. In our case EM played the crucial role in driving migration since the temperature gradient between chip side and substrate was not extremely high (estimated 800 °C / cm).

The cumulative distribution of failure data for die with 60 µm solder balls on PCBs are illustrated in figure 13. The time to failure data appear to follow a Weibull distribution quite closely for all test conditions.

![Graphs showing Weibull distribution of EM lifetime data for chips with SAC305 solder bumps with 60 µm diameter on PCB with ENIG finish at 125 °C oven temperature.](image)

Fig 13: Weibull plots of EM lifetime data for chips with SAC305 solder bumps with 60 µm diameter on PCB with ENIG finish at 125 °C oven temperature, left diagram for 8 kA/cm², right diagram for 5 kA/cm².

At 125 °C oven temperature and 5 kA/cm², 63.2 percent of the chips failed within 1246.98 hours, at 8 kA/cm², 63.2 percent of the flip chips failed within 120.17 hours, indicating temperature is an especially damaging factor.

The most benign testing condition (28 °C ambient temperature, see table 2, has resulted in zero failures during 8000 hours test time, as expected. The failure data from the other EM tests can be used to determine the parameters of the modified Black's equation [6]:

\[
MTTF = A \cdot J^n \cdot \exp\left(\frac{E_a}{k \cdot T_{bump}}\right) \quad (1)
\]

Once the mean time to failure (MTTF) is determined in this empirical relationship with the EM tests according to table 2, the constant A, the current density exponent n, and the activation energy \(E_a\) can be determined, as described in [7] and [8].
The current carrying capacity for a certain operating life time (for instance 100,000 hours \(= 11.4 \text{ years}\)) and failure rate can be determined using the method outlined in [7] and [8]. Designers need to take into account maximum allowable current per solder joint for a given operating temperature and lifetime requirement. The projected lifetime and allowed currents are best used with some caution when assessing a product with the same design and material composition as the test vehicle.

**Discussion**

Ductile SnAgCu solder material in the center of the solder joint [1], see figure 5, 7, and 9, and high performance underfill [3] contribute to good reliability during temperature cycling. The solder alloy in those very tiny solder bumps makes EM testing mandatory, as high current densities and high temperatures are expected. Work performed by other authors shows that EM performance can be improved by transforming Sn into tin-copper intermetallics (IMCs) [9]. If, as in our experiments, parts with large CTE mismatch are used, thermal cycling performance would decrease dramatically due to the low ductility of the intermetallic compounds [10].

One significant problem is that EM is influenced by a wide variety of physical phenomena and depends on a large number of intrinsic and extrinsic effects. [11] Errors in lifetime estimation arise from the assumption that the fitting parameters \(A, n, \) and \(E_a\) obtained from the accelerated EM tests can be directly applied for the lifetime extrapolation without consideration of additional temperature due to Joule heating and pre-existing stress dependencies [4].

For solder bump interconnects with current crowding, electromigration will follow the peak current density as can be concluded from figure 11 and figure 12. In addition to that, the underfill material above the glass transition temperature \(T_G\) has different properties than below \(T_G\) which might have an impact on the lifetime of the flip chip assemblies as well.

**Summary and Conclusion**

It is clear that characterizing EM is a rather complex and challenging task [4]. The results indicate: Current density and particularly bump temperature are the most important drivers during EM testing. The failure progress by current stressing can be divided into three phases: First, the incubation time with vacancy accumulation [12]. Second, the decrease of contact area at the cathode side occurred by solder depletion and/or void formation and growth where current crowding was present. Third, after reduction of contact area, the solder joint degraded seriously - presumably due to resistance increase and self-heating, accelerating the EM (and likely TM) of solder. And finally, at least in some cases, causing the solder to melt [13], and then the solder joint was electrically opened.

Solder joints with 50 \(\mu\)m, 40 \(\mu\)m bumps or 30 \(\mu\)m bumps on thin film ceramic showed low degradation during EM testing due to lower bump temperatures because ceramic distributes the heat very well. Voids did not form at the cathode interface during the first 1000 hours, only intermetallic compound (IMC) dissolution and metallization consumption was observed.

This work established the importance of measuring the actual temperature very close to or underneath the solder bump preferably at the chip side and the substrate side in order to understand the EM and thermomigration behavior better. As a general assumption, our test data are sufficient to provide an overlook of the EM performance of the solder connections.

In conclusion, the investigated test coupons with ultra fine-pitch flip chips employing SAC305 solder spheres with diameters down to 30 \(\mu\)m have a sufficient reliability and electromigration lifetime for most applications.

**Future developments**

PCBs in semi-additive or additive technology could enable further miniaturization of pitch and bump size and resins with lower CTE enhance temperature performance further [14].

Lifetime under EM stress conditions presumably can be enhanced using alternative UBM materials like Co-W [15] or specialty solder alloys [16].
References


Presented by:
Micro Systems Engineering, GmbH
Schlegelweg 17
DE-95180 Berg
Germany

For further information, please contact:
Kevin Walker
Micro Systems Technologies, Inc.
E kevin.walker@mst.com
P 480-398-1496